

A Next-Generation Pentium® III Processor with Performance Optimizations

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Product Overview

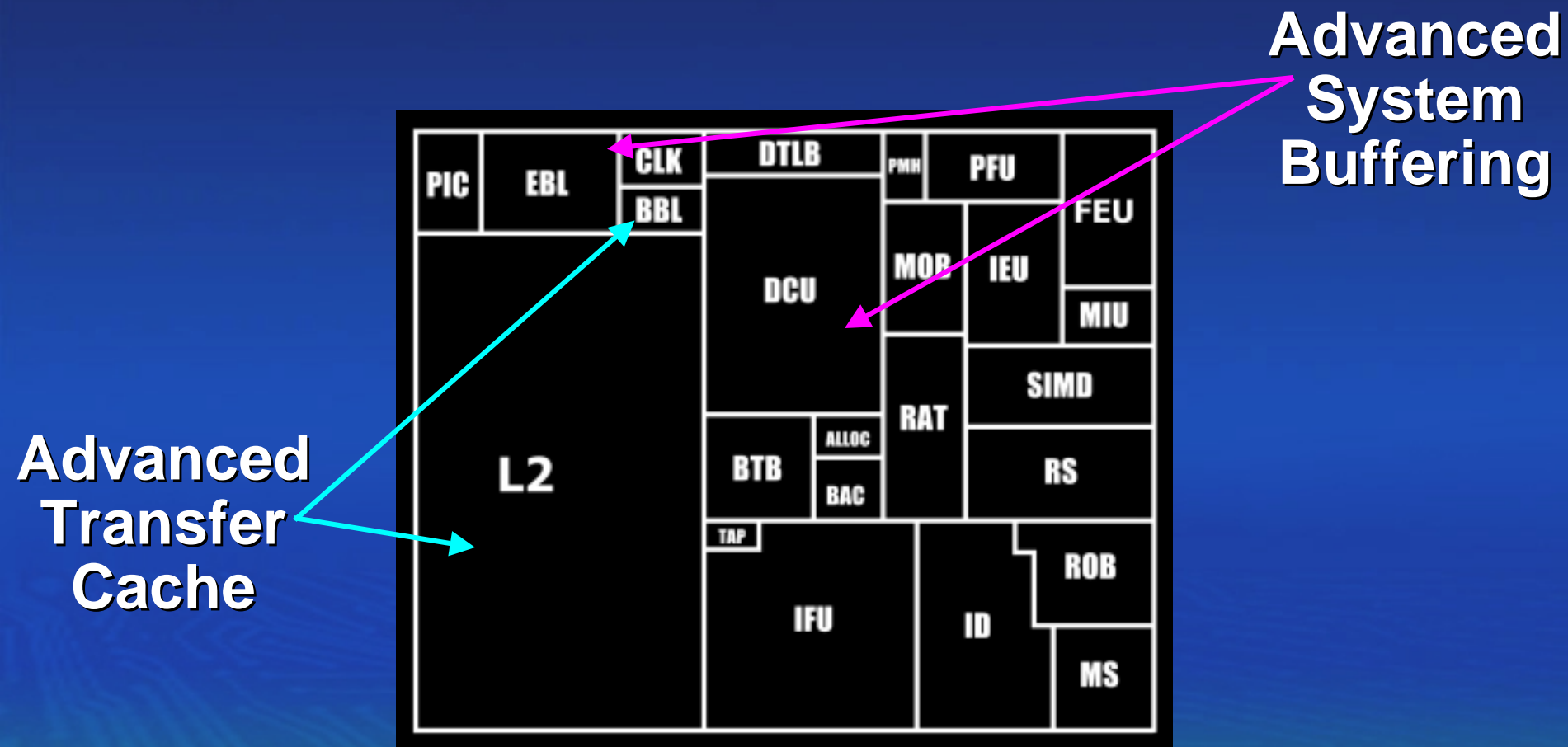
- Pentium® III processor core
- 700 MHz or greater at launch
- Advanced Transfer Cache (ATC) - 256KB on-die
- Advanced System Buffering (ASB)
- Intel® SpeedStep™ technology (for mobile)
- 0.18μ process
- 6 metal layer process
- 28 million transistors
- 106 mm² die size
- Slot, socket and mobile package options
- Multi-voltage capability: 1.1V-1.7V
- On-die GTL+ termination

Design Goals

- Optimally utilize Intel's 0.18 μ semiconductor process for rapid, high volume ramp
- Provide significant performance improvement at given frequency
 - Level 2 cache enhancements
 - System bus bandwidth optimizations
- Assure frequency headroom
 - Full chip re-layout to utilize extra metal layer
 - Remove RC-limited critical paths
- Achieve cost reductions and enable new form factors
- Design for mobile, desktop, server & workstation segments

Higher Performance at any MHz

Key Areas Of Design Focus



Layout optimized for 0.18 micron process

Advanced Transfer Cache

- **Size**
 - 256KB on-die level 2 cache
- **Organization**
 - 8-way set associative, 1024 sets
 - 32 byte line (32 bytes data, 4 bytes ECC)
 - 36-bit physical address space
- **Latency**
 - >4x reduction in latency (as compared to today's Pentium® III processor)
- **Cache Bus**
 - Full speed, scalable with core frequency
 - 288-bit transfer width (256 data, 32 ECC)
 - 2 cycle back-to-back throughput
- **Manufacturability**
 - Programmable BIST
 - Redundancy
- **MESI protocol maintains cache coherency**

Heavily Integrated and Highly Optimized

Advanced Transfer Cache Performance Benefits

- **Bandwidth** (256-bit data, 2 clock back-to-back throughput)
 - 32 Bytes every 2 clocks (11.2GByte/s @700MHz)
 - Scalable with core frequency
 - Enables full system bus utilization
- **Latency** (> 4x improvement in L2 latency)
 - Decreases penalty of L1 cache misses
 - Reduces snoop stalls >20x compared to today's Pentium® III Xeon™ processor
- **Associativity** (8-way set associative, 1024 sets)
 - Increases performance of cache for real applications
 - ~3% benefit for integer, business and workstation workloads
 - ~6% benefit for server oriented workloads(TPC-C)

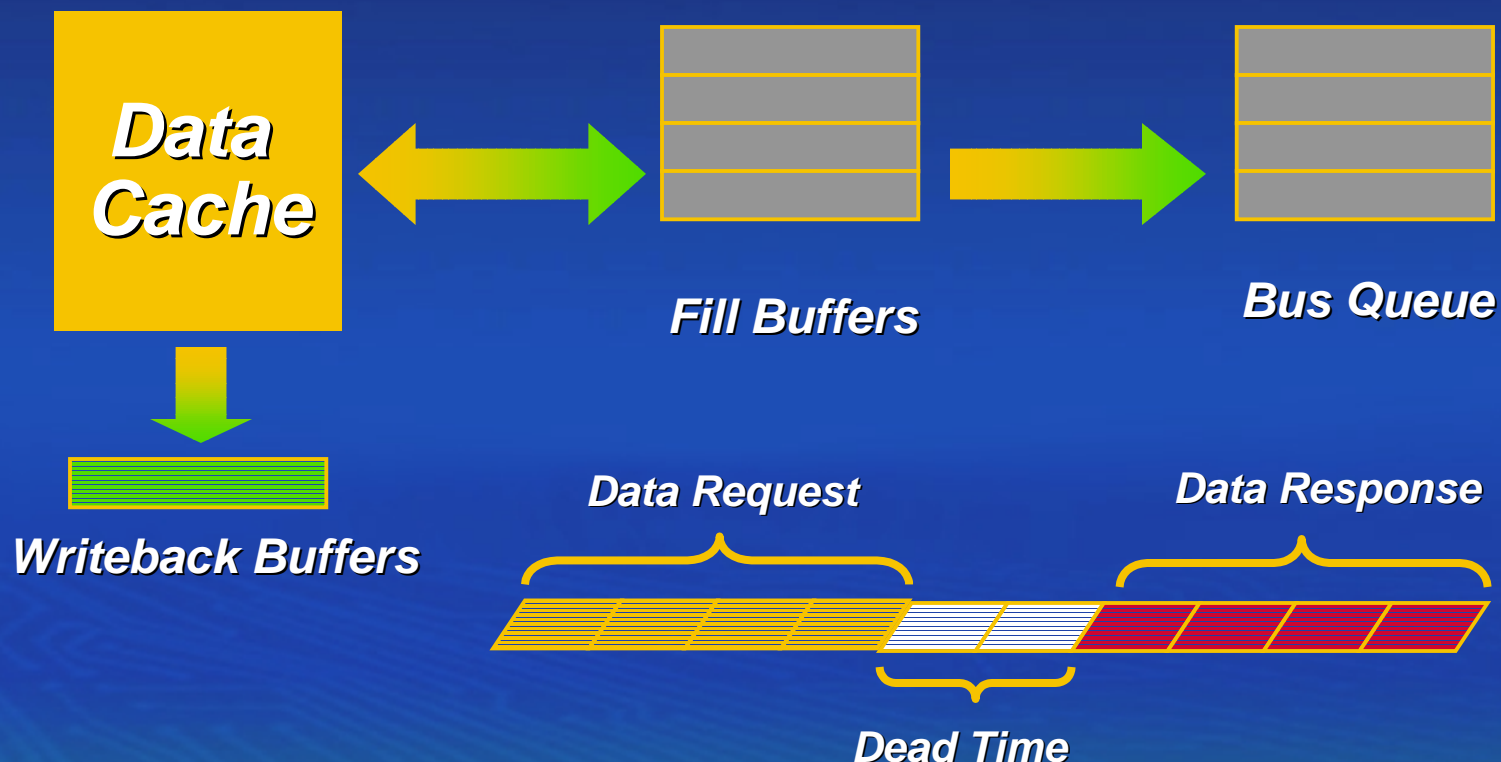
**ATC Performance
Scales with Core Frequency**

Advanced System Buffering

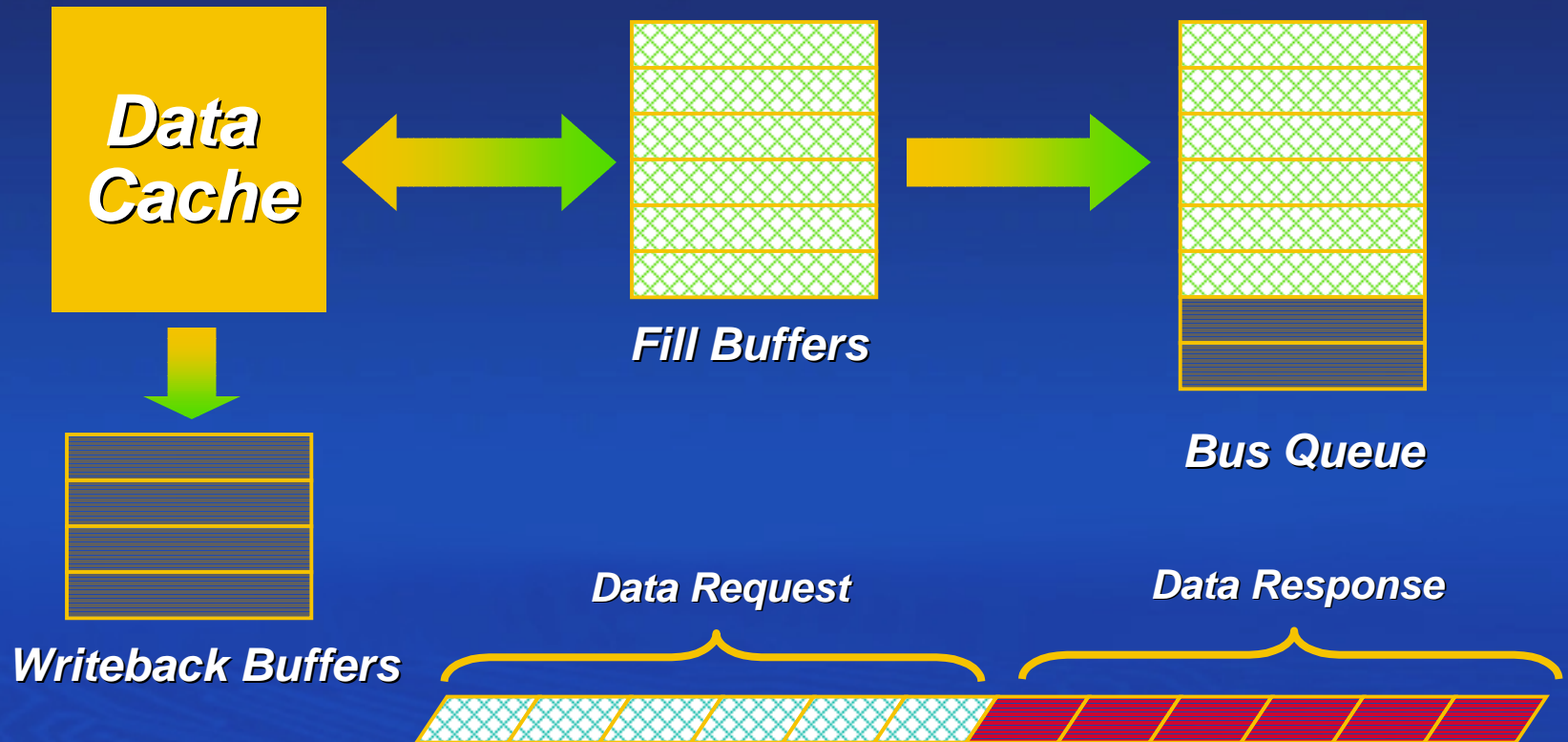
- **Balanced increase in buffers to minimize bottlenecks**
 - Buffer sizes maximize utilization of the 133MHz system bus bandwidth
- **6 Fill buffers (increased from 4)**
 - 50% increase in concurrent non-blocking data cache operations
- **8 Bus queue entries (increased from 4)**
 - Allows more outstanding memory/bus operations
- **4 Writeback buffers (increased from 1)**
 - Reduced blocking during cache replacement operations
 - Faster deallocation time for fill buffers

System Bus Interface Optimized for 133MHz

Non-optimized Buffering



Advanced System Buffering Bandwidth Utilization

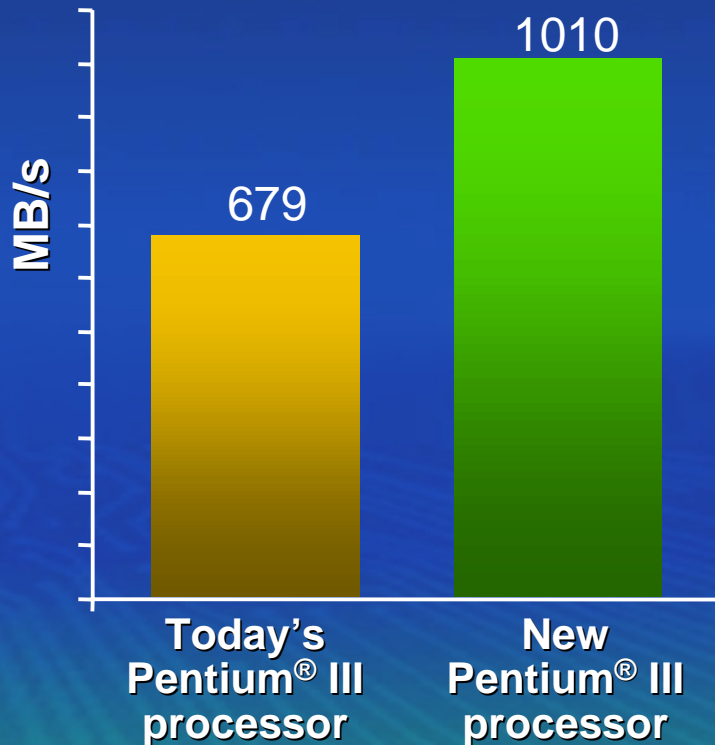


Allows >1.0 GB/S
Sustained BW on 133MHz System Bus

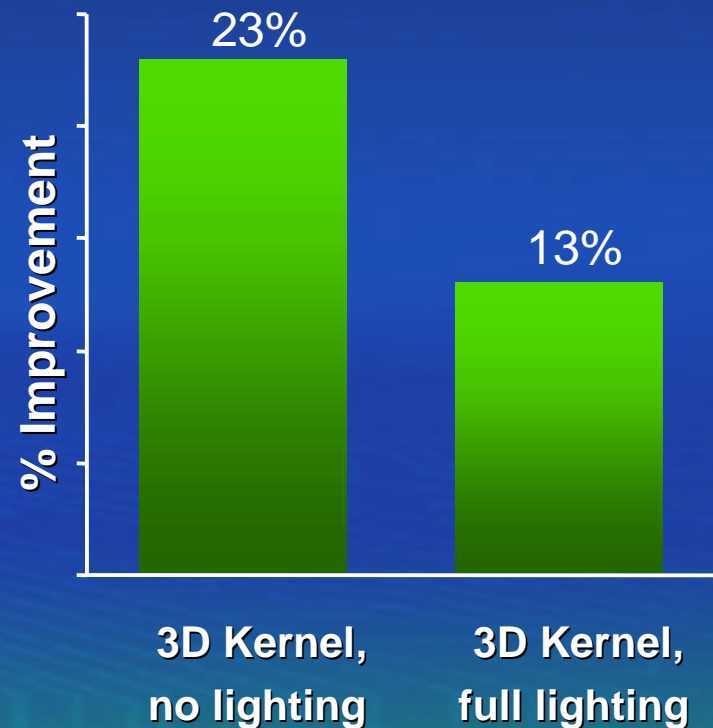
Performance Analysis

Comparing Processors at 600MHz with 133MHz System Bus

Memory Bandwidth Prefetch



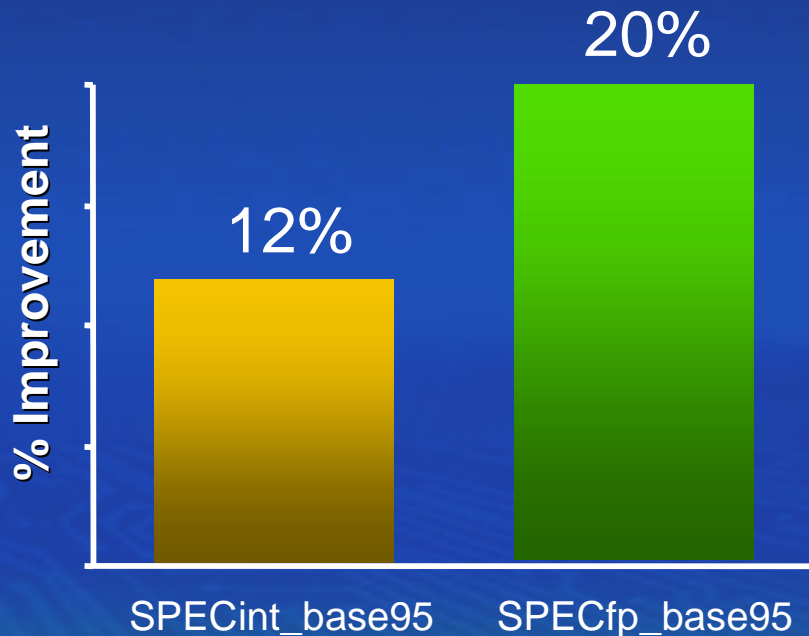
Memory Bound 3D Performance



New Pentium III processor 600 MHz (with ATC, ASB) vs. today's Pentium III processor 600 MHz
System configuration: Pre-production Intel VC820 board with 133 MHz system bus, 128MB RDRAM, Seagate Barracuda SCSI, STB4400 Velocity AGP 2X. Intel internal design analysis tools used to obtain measurement data.

New Design Achieves Improved Performance Goals

Performance Gain at Equal MHz (600MHz)



- Improved handling of large floating-point data sets
- Estimated results for **NEW Pentium® III** processor at 600 MHz
 - SPECint_base95: **29**
 - SPECfp_base95: **25**

Frequency Headroom

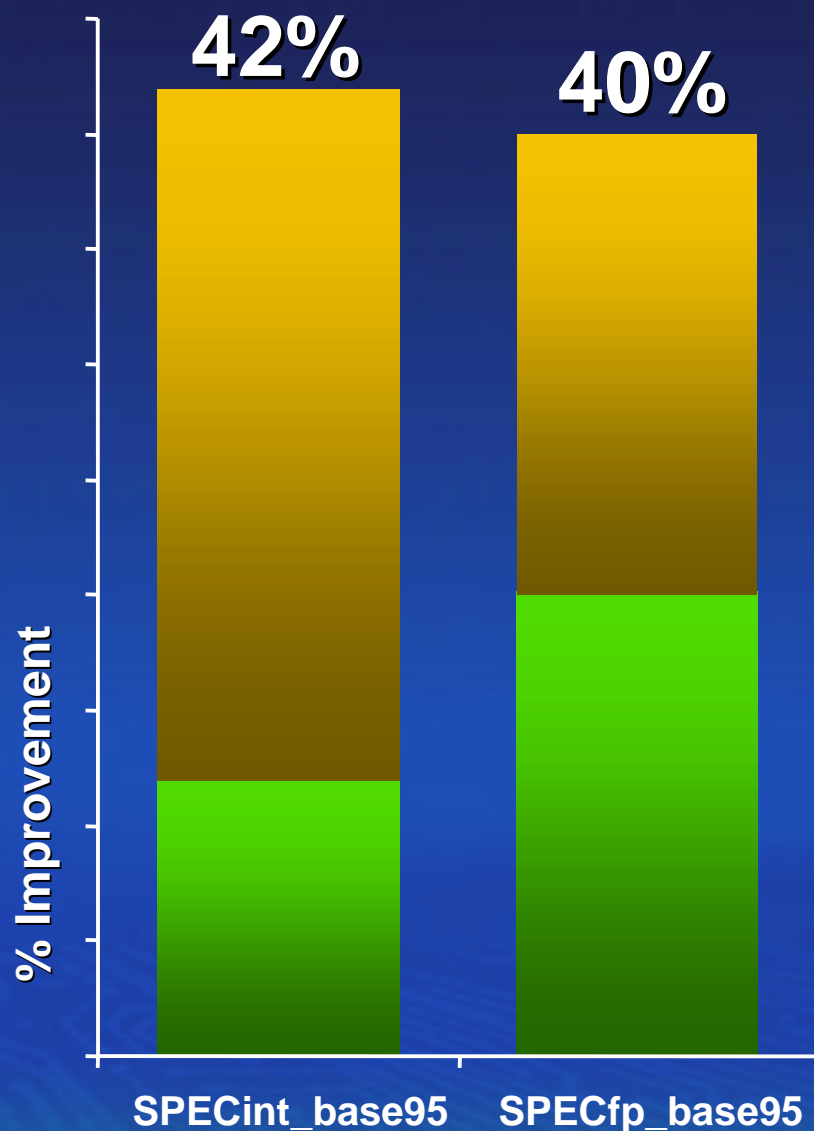
- 0.18 μ process

- Decrease in minimum gate dimension for improved transistor speed
- Fluorine-doped SiO₂ (SiOF) dielectric for reduced capacitance resulting in global speed
- Additional metal layer for routing density
 - Enables full-speed integrated L2 interface

- Design for RC

- Design interconnect simulated at more than 200MHz above target frequency
- Cross-capacitance effects extensively simulated and accounted for within design
- Optimized for future transistor improvement

Designed for Frequency Scalability



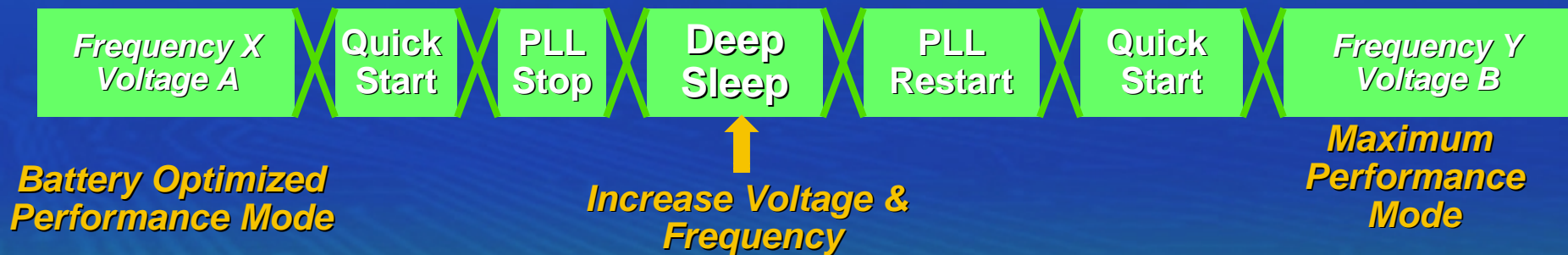
**Performance
scales to 800MHz
and beyond!!**



New Pentium III processor 800 MHz (with ATC, ASB) vs. today's Pentium III processor 600B MHz
Source: Intel MAP; Results estimated using Intel C/C++ Compiler 4.5 and Intel Fortran Compiler 4.5
System configuration: Pre-production Intel VC820 board with 133 MHz system bus, 256MB RDRAM,
IBM371800 ATA-66, Diamond Viper 770 Ultra TNT2 AGP4X

Mobile Features

- 1.1V-1.6V operation capability for all types of mobile applications
- Intel® SpeedStep™ technology – provides automatic switching of frequency and voltage based upon a power source change
- Two Performance Modes
 - Maximum performance mode: highest-frequency and voltage when connected to external power
 - Battery optimized performance mode: maintains 80% of maximum performance at 50% of the power when running on battery



Summary

- Great MHz-to-MHz performance improvement driven by **Advanced Transfer Cache** and **Advanced System Buffering**
- High volume 0.18μ process manufacturing already in production
- Design has frequency headroom for the future
- Product will volume launch into Mobile, Desktop, Workstation and Server segments